WRITEBACK AND REFRESH CIRCUITRY FOR DIRECT SENSED DRAM MACRO

Abstract of the Disclosure

A writeback and refresh circuit for a direct sense architecture memory wherein a plurality of primary sense amps are connected to a global data line and also to bitlines, each of which is coupled to an array of memory storage cells which are selected for write and read operations by a plurality of wordlines. A single secondary sense amp receives analog level data from the primary sense amps over the global data line, and includes a restore/writeback circuit which digitizes the data and then returns the digitized data over the global data line to the primary sense amp and back into the memory. A 2-cycle read/writeback operation is used for each memory read cycle, a first cycle read operation, and a second cycle writeback operation. The 2-cycle destructive read architecture eliminates the need for a cache and complex caching algorithms.

Figures